Claims

We claim:

1. A method for etching a capacitor comprising the steps of:

depositing a hardmask on a top electrode of a capacitor stack comprising a ferroelectric layer sandwiched between the top electrode and a bottom electrode;

etching at a first temperature to pattern the top electrode according to the pattern of the hardmask;

etching at a second temperature lower than the first temperature to pattern the ferroelectric layer according to the pattern of the top electrode and resulting in the top electrode having sidewalls beveled relative to a top surface of the top electrode; and

etching at a third temperature to pattern the bottom electrode to form the capacitor.

2. The method of Claim 1, further comprising the step of encapsulating the capacitor with a second hardmask prior to patterning the bottom electrode.

3. The method of Claim 1, wherein the patterning of the bottom electrode further comprises using the top electrode to pattern the bottom electrode.

4. The method of Claim 1, wherein the top electrode is comprised of Pt and the first temperature is between 250 and 400 degC.

5. The method of Claim 1, wherein the second temperature is less than the first temperature by between 50 and 100 degC.

6. The method of Claim 1, wherein:

the etching at the first temperature to pattern the top electrode according to the pattern of the hardmask is performed in a first etching chamber; and

the etching at the second temperature lower than the first temperature to pattern the ferroelectric layer according to the pattern of the top electrode is performed in a second etching chamber having a temperature lower than the first chamber

7. The method of Claim 1, wherein the third temperature is substantially the same as either the first temperature or the second temperature.

8. A capacitor comprising:

a substrate;

a bottom electrode supported by the substrate; and

a ferroelectric layer sandwiched between the bottom electrode and a hardmask top electrode, the top electrode having sidewalls beveled relative to a top surface of the top electrode due to use of the top electrode as a hardmask for etching the ferroelectric layer of the capacitor.

9. The capacitor of Claim 8, wherein the hardmask top electrode is comprised of a noble metal.

10. The capacitor of Claim 9, wherein the hardmask top electrode is comprised of Pt.

11. The capacitor of Claim 8 wherein the ferroelectric is comprised of PZT.

12. The capacitor of Claim 8, further comprising a second hardmask encapsulating the capacitor.

13. The capacitor of Claim 12, wherein the second hardmask is comprised of TEOS.

14. The capacitor of Claim 8, wherein the top electrode is etched at a first temperature so that the top electrode has a pattern of a overlying hardmask; and the ferroelectric layer is etched at a second temperature lower than the first temperature so that the ferroelectric layer is patterned according to the pattern of the top electrode and so that the top electrode sidewalls beveled relative to a top surface of the top electrode.